Chip Scale Package Burn-In Socket Technology as Pitches Move to 0.5 mm

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Abstract

The growth and miniaturization of consumer electronics, and the drive for increased capability inside a smaller package, has resulted in the development of chip scale packages. These new smaller formats are gaining acceptance and the back end assembly and test infrastructure is meeting the challenge of contacting these devices.

To ensure reliability a number of memory devices still require burn-in to eliminate early product failures before the devices are sold and assembled into the end product. This requires upgrading the burn-in infrastructure including test boards and socket technology to meet the pitch and I/O requirements of the new packages. Burn-in sockets must satisfy a number of requirements and the socket design community has been challenged to conceive and create new contacting systems.

This paper will review some of the benefits of Chip Scale Packages and illustrate some of the devices currently available. The difficulties of contacting solder balls will be discussed and examples of how these challenges have been met provided. The differences between sockets for high and low volume requirements will be highlighted.

The potential for pitches less than 0.5mm will be discussed and some of the techniques currently being evaluated presented.

Introduction

The very first semiconductor device built in Bell Labs by Bardeen and Brattain for Shockley was not packaged. The fragility of the device required that it be protected from the outside world and thus the semiconductor packaging industry was born. Since that day in December 1947 the wizards of the semiconductor world have continued to reduce the size of the transistor so that more power can be packed into the same space and Moore's[1] Law, or rather prediction was created. The packaging engineers, who initially used metal cans to protect the transistor, moved to ceramics and molded plastics as device complexity increased. They have kept step with this revolution and have provided an alphabet soup of packages ranging from the early "cans" through the DIP (Dual In-line Package) to the CPGA (Ceramic Pin Grid Array), the BGA (Ball Grid Array) to the latest - CSP's, Chip Scale Packages.

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[1] Moore's Law is attributed to Gordon Moore, one of the "Traitorous Eight" from Shockley Semiconductor who went on to found first Fairchild Semiconductor and then Intel who, in 1965 observed that ..... *"the amount of data that a microchip can hold doubles every year or at least every 18 months".*

The important characteristic is smaller and the packaging engineer is responsible for a providing environmental protection while also providing electrical connection to the outside world. The size of the packaged device is often 2 to 10 times larger than the actual chip. The recent development of hand held/portable devices such as camcorders, cell phones and palm computers requires a smaller package format and these “Killer Apps” gave birth to the Chip Scale Package.

A CSP is a surface mount package and is typically defined by the size of the package being less than 1.2 times the size of the die. The connection to the outside world is normally solder balls, although there are some packages such as the BCC which have pads. The pitch of the solder balls is between 1.0 to 0.75 mm and this has created a number of challenges for the designers and assembly of the socket. This paper will review the need for burn-in sockets and how the socket industry has responded to the requirements of the burn-in community.

The challenges of socketing the next generation of devices with pitches of 0.5mm and less will be reviewed and some of the potential solutions discussed.

Reliability and the Need for burn-in

The creation of any product involves a number of different process or manufacturing steps. Since these steps are subject to some variability, no matter how small, there is the opportunity that the final product will have some small defect which will cause it to fail prematurely. The reliability engineers are familiar with this and all products have a failure rate versus time curve similar to that shown in figure 1, known as the “Bathtub Curve”.

The phases of product reliability can be broken into three phases ....

1. Early failures or “Infant Mortality” as a result of some processing or manufacturing defect.
2. Normal operating life where failures are the result of some “random” event.
3. Wear out when the product has reached the end of its useful life and various components begin to break.

The early life failures can be high when a process is at the leading edge of technology and the ability to find the right recipe or stable process conditions takes time. To reduce the potential for selling defective components the product is tested to eliminate these defects. This process can be accelerated by intentionally stressing the components to force the early failures. In the semiconductor industry this process is known as “burn-in “ and devices are stressed using extremes of temperature and voltage with the objective of forcing the failure so that the defective device can be sorted and scrapped.

Socketing Challenges

Burn-in is achieved by placing the package in a socket which provides a temporary contact to the I/O. This socket must satisfy a number of performance requirements including:

- The contacts must provide reliable electrical connection so that there is no possibility of a loss of continuity. A momentary loss of continuity will be interpreted by the burn-in monitors as a “fail” and the device will be rejected.
- The contacts must not damage the I/O of the package which for many CSP’s is a soft solder ball. At burn-in temperatures of 125 to 150ºC contacting a solder ball can be difficult since the solder can “stick” to the contact.
- The contacts must be robust so that it works reliably over the repeated cycling and high temperature excursions associated with multiple uses.

The ways in which socket manufacturers have solved these challenges have been described in a number of different articles and papers [1-3]. The key issues are discussed in greater depth below with particular emphasis on the challenges facing the socket designers as package pitches move to 0.5mm.

The 0.75 mm Solution.

A is schematic of some of the different techniques to contact the solder ball is shown in figure 2. One of the concepts which has received broad acceptance for pitches of 0.75mm and greater is the dual pinch style shown in figure 2(a). This contact has the advantage that it grips the sides of the solder ball and does not damage the bottom of the solder ball. An SEM photograph of a dual pinch contact is shown in figure 3 which also includes a photograph of the probe mark on the solder ball after burn-in.

In the operation of the socket one or both of the contact arms move aside to allow the package to fit into the socket. With the contacts open the package is placed in the socket and, as the socket closes, the contact arms close onto the solder ball. The contact force is established by the specific geometry and design of the contact arms and the material of construction. Beryllium copper has been the alloy of choice for spring applications because of its electrical conductivity and good stress relaxation characteristics when exposed to high temperatures.

When loading the package it is essential that there is sufficient space for the contact arms to open wide enough to accommodate the tolerances of the ball diameter and the ball location. A schematic of the available space is shown in figure 4 for a 0.75mm pitch array of 0.35mm diameter balls. This schematic illustrates that space is at a premium – even when the material thickness for the contacts is 0.12 mm or 0.0047”. One way to increase the available space is to actuate the socket at 45º to the axis of the array. The available space using this approach is shown schematically in figure 5 which indicates that the distance between the contacts has increased 3 times from 0.16 mm to 0.47 mm. The realization of this concept is shown in the socket shown in figure 6.

The 0.5mm Space Problem

The methodology used to gain space to assemble and actuate the contacts in sockets for the 0.75mm pitch array cannot be used for 0.5mm. The situation is shown schematically in figure 7. Illustration (a) shows that when arranged

parallel to the axis of the socket the contacts will interfere with each other; illustration (b) shows that the space between the solder balls even at 45º to the axis of the array is only 0.17 mm or 0.007". The difficulty of molding parts with walls and features of this size and the stamping and forming of the beryllium copper at thickness' less than 0.12mm thick has been solved but is not economical on a commercial scale. Several ideas and concepts are being evaluated however no product has been announced which uses the pinch style contact at a pitch of 0.5 mm.

A Solution for 0.5mm Pitch Devices

Alternate approaches for contacting the solder balls have been suggested and include some of those shown in figure 2. The majority of effort to-date has been focused on the use of a contact which uses the space under the ball for actuation rather than the space at the side; that is the contact moves vertically. These types of contacts which include spring elements and pogo pins are shown schematically in figure 8. These contacts need a vertical load to be applied to the package and this is accomplished using a clamshell type socket rather than the preferred open top style. The open top type is favored for high volume applications because of ease of use with automated equipment for loading and unloading the sockets.

One of the solutions for 0.5mm pitch devices uses a spring to contact the solder ball. The fabrication of such springs requires specialized equipment, knowledge and capability and while difficult has been achieved as shown in figure 9. This spring has been incorporated into a carrier and sockets using this technology are being qualified at major semiconductor manufacturers. This particular spring can be thought of as two springs – the top half acts to contact the solder ball – the bottom half provides a compression mount to the burn-in board. Since the spring is held at the middle by the carrier each half of the spring acts independently of the other. This allows the contact to the burn-in board to establish a gas tight seal when the socket is mounted onto the board. This contact is not broken each time the socket is unloaded. Because the carrier is a separate component it can be thought of as a "contractor" and it is possible to replace this part if the original is damaged during test.

The socket and a close up of part of the array of springs is shown in figure 10. A cross-section through the socket is shown in figure 11. Each spring makes contact with a single solder ball. The individual solder balls nestle into the inner diameter of the spring and this wiping action establishes the electrical contact. During burn-in the solder becomes extremely soft and the spring will imprint on the solder ball. Typical solder ball contact marks after exposure to 150º for 6 hr. are shown in figure 12. This probe mark is considered acceptable. At lower temperatures the probe mark would not be as obvious. This socket is currently being evaluated and additional information will be published when it is available.

The Future

The need for increased functionality in a smaller package continues to drive the move toward smaller pitch I/O and ultimately flip chip. Berry and Winkler[4] of

Electronic Trend Publications have reviewed the pitch issues for area array packages. They point out that Japanese assemblers have worked with conventional leaded packages with pitches of 0.3 mm while most US assemblers have been reluctant to handle devices with pitches below 0.5mm. However the need for high I/O count logic devices, in a small form factor, will drive the move to pitches below 0.75 mm. Berry and Winkler forecast that in 3 years the annual use of CSP devices with pitches less than 0.5mm will be more than 2 billion - a compound annual growth rate of 191%.

It is clear that the move to pitches of 0.5 mm and less is inevitable. The challenges of test and burn-in will require the development of some novel socket concepts and new contacting techniques.

Summary

The semiconductor industry continues to provide more in less space and the development of the Chip Scale Package is the latest format. Burn-in testing of these devices has resulted in the development of new types of miniaturized contacts for pitches greater than 0.75 mm. These sockets have been accepted and users are now purchasing significant numbers of sockets for the burn-in testing of memory die. The move to 0.5 mm pitch packages is challenging suppliers to develop new types of contacts. Some of the alternates have been reviewed and one type, involving the use of a spring has been described. This socket is being qualified at a major semiconductor manufacturer.

The ability of the mechanical world to make sockets will be further challenged every day as the manufacturers of silicon push the size down and the performance up.

Acknowledgments

The author would like to express his thanks and appreciation to all the design and manufacturing teams within Texas Instruments Interconnection Business Units in the USA, Japan and Korea who have worked to translate the CSP sockets concepts into functional and reliable products.

References

1) Akram, S.; *"Socket contacting technology trends for flip chip and chip scale packages"*, Future Fab 2000, Vol. 8 pp. 301-303,
2) Crowley, R.T.; "*Chip scale packaging: Technology analysis and market forecast*", pub. Redpoint Research, Feb. 1998.
3) Forster, J. A.; *"Performance drivers for fine pitch BGA sockets"* Proceedings the Technical Conference at Chip Scale International-98, pp127-131, pub by IPC 1998.
4) Berry, S. and Winkler, S.; "Area Array Package I/O Pitch will Continue to Decline" Chip Scale Review, Vol. 4, No. 2, pp. 9, March-April 2000

Biography

A technology manager within Texas Instruments' Interconnection business, Dr. Forster oversees the CSP, KGD, and PGA burn-in test socket technology programs. He has over twenty-one years of experience in the materials development field working on concepts for the contacts used in burn-in sockets, materials selection, thermal management issues and new product development. Past activities at TI have included managing an R&D group focused on developments in clad metals, insulated metal substrates, and metal matrix composites. Dr. Forster has authored more than 25 technical publications including several on the challenges of burn-in sockets for chip scale packages.

A holder of more than fifteen U.S. patents, Dr. Forster was educated in England receiving a B.Sc. (Hon.) from the University of Manchester Institute of Science and Technology. He earned his doctorate in mechanical engineering at McMaster University in Hamilton, Ontario, Canada.

Figures

Figure 1: The bathtub curve showing the phases of a product life

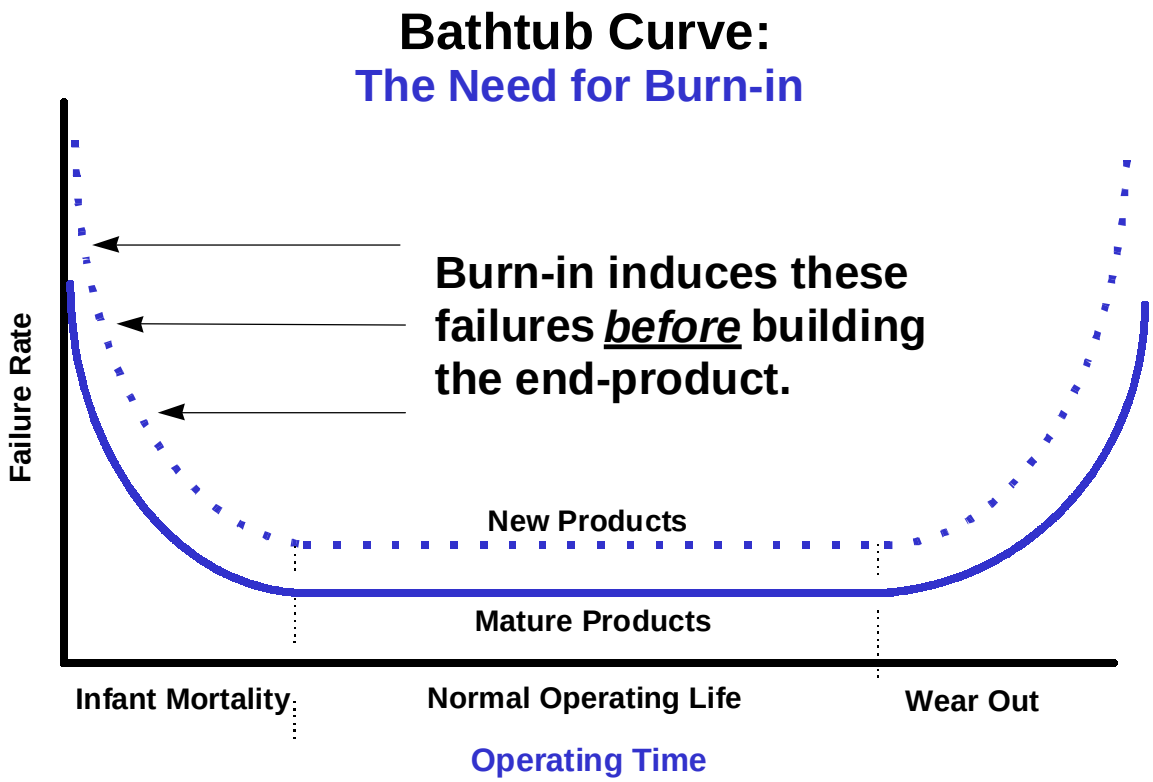


Figure 2: Schematic of some of the different techniques to contact a solder ball.

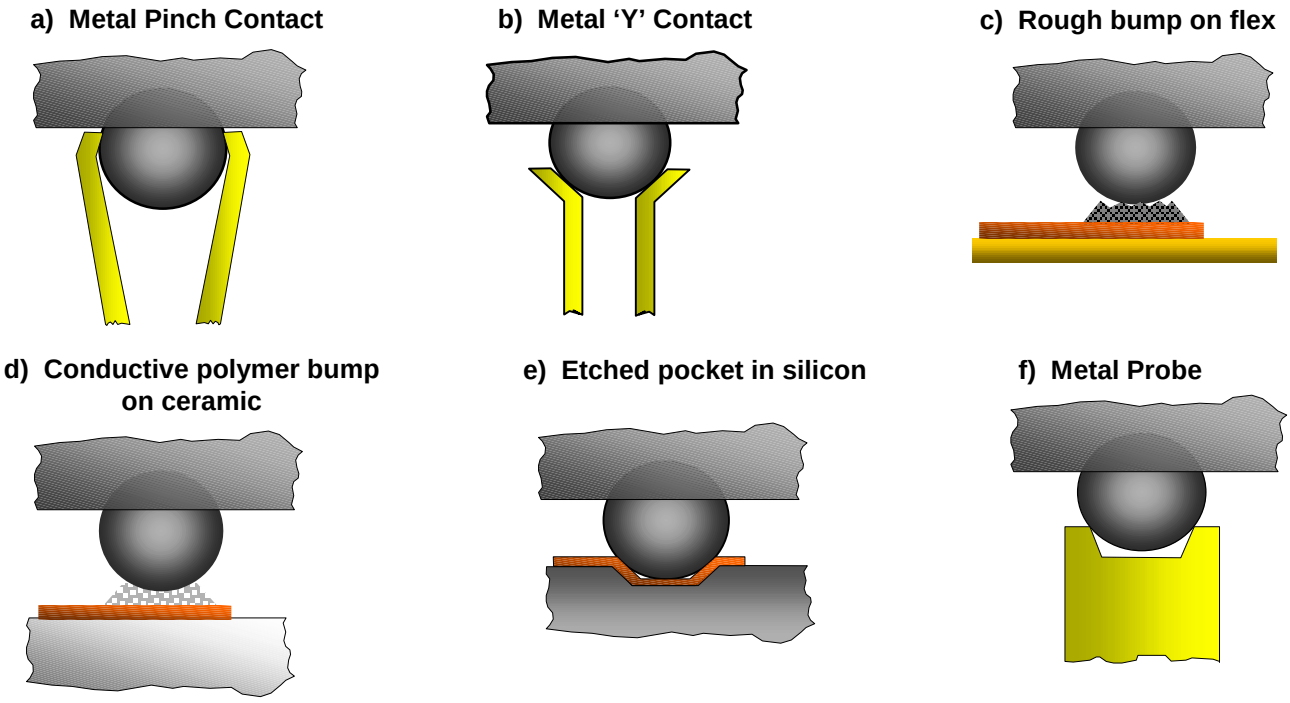


Figure 3: Dual pinch contact used for contacting a solder ball

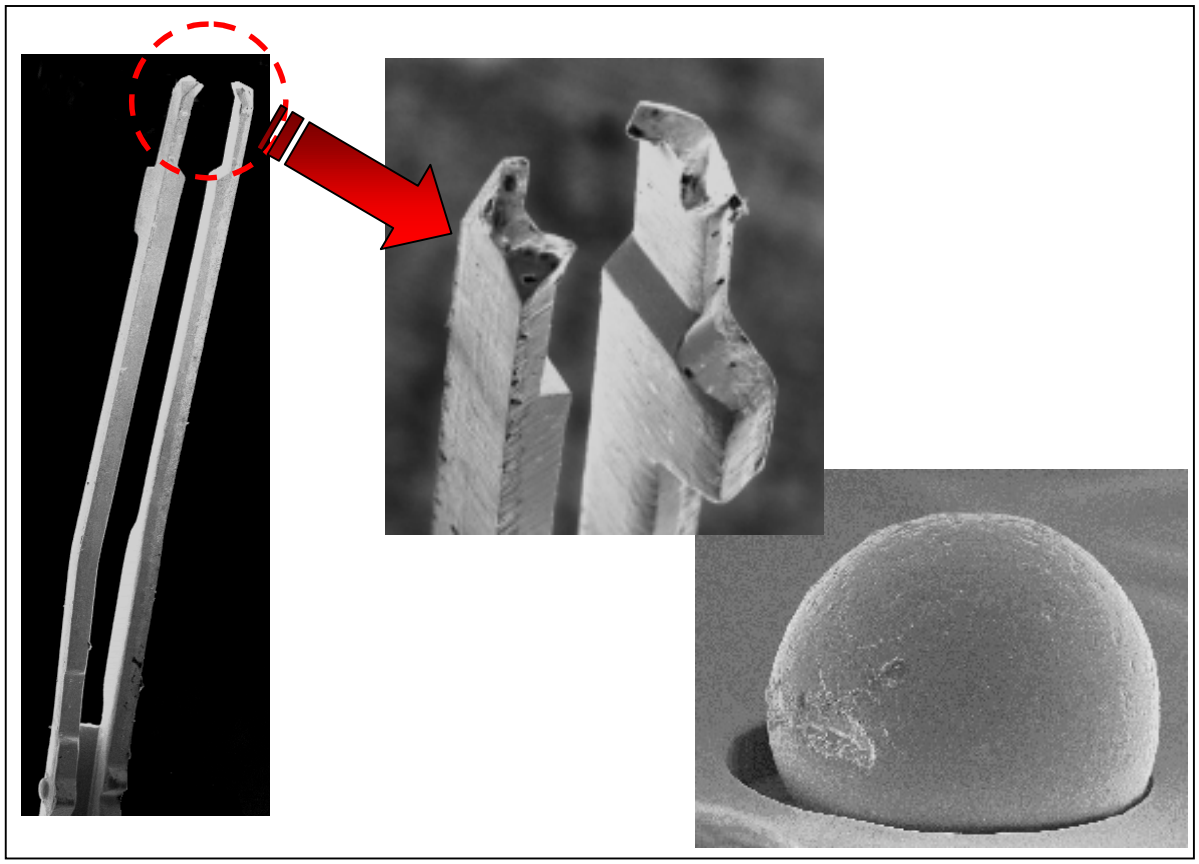


Figure 4: Schematic of the available space for actuation of the contact for a 0.75mm pitch array;
Solder ball dia. 0.35mm Contact thickness 0.12mm.

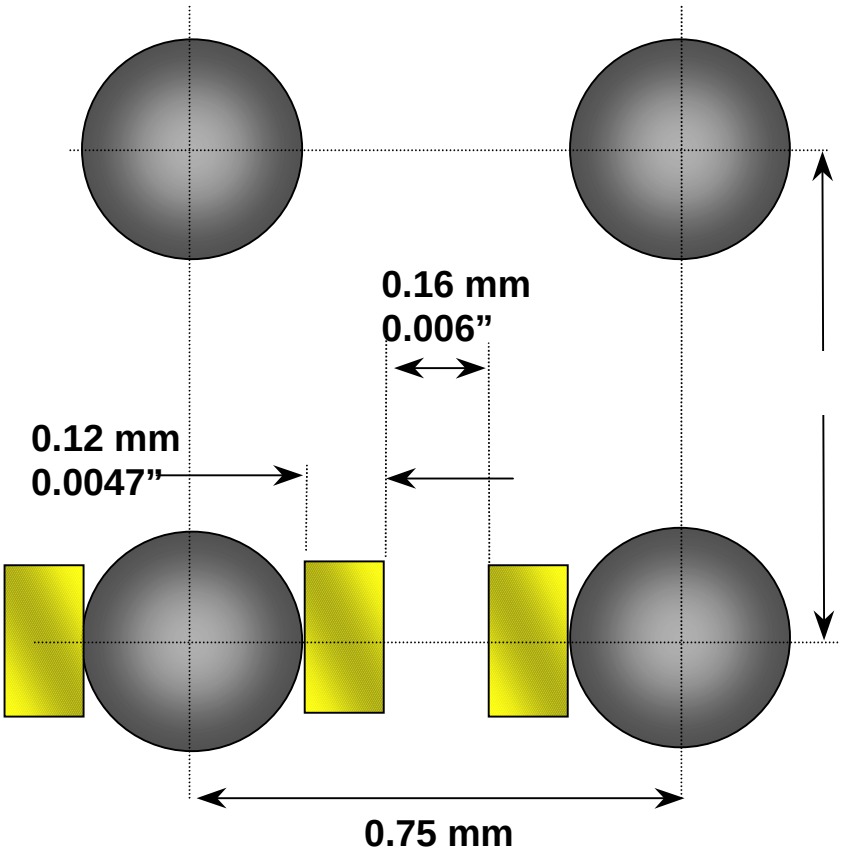


Figure 5: Schematic of the available space for actuation of the contact for a 0.75mm pitch array; Actuation at 45º to axis of array.
Solder ball dia. 0.35mm Contact thickness 0.12mm.

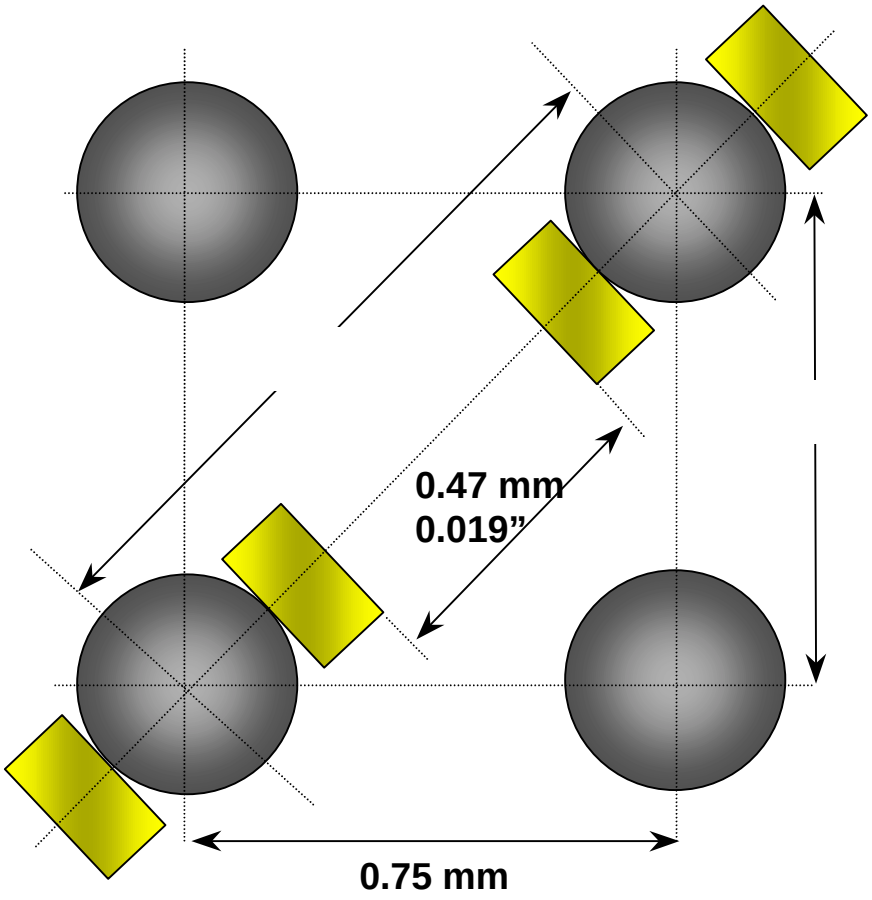


Figure 6: CSP Socket which is actuated at 45º to axis of array to provide more space for contacts to open

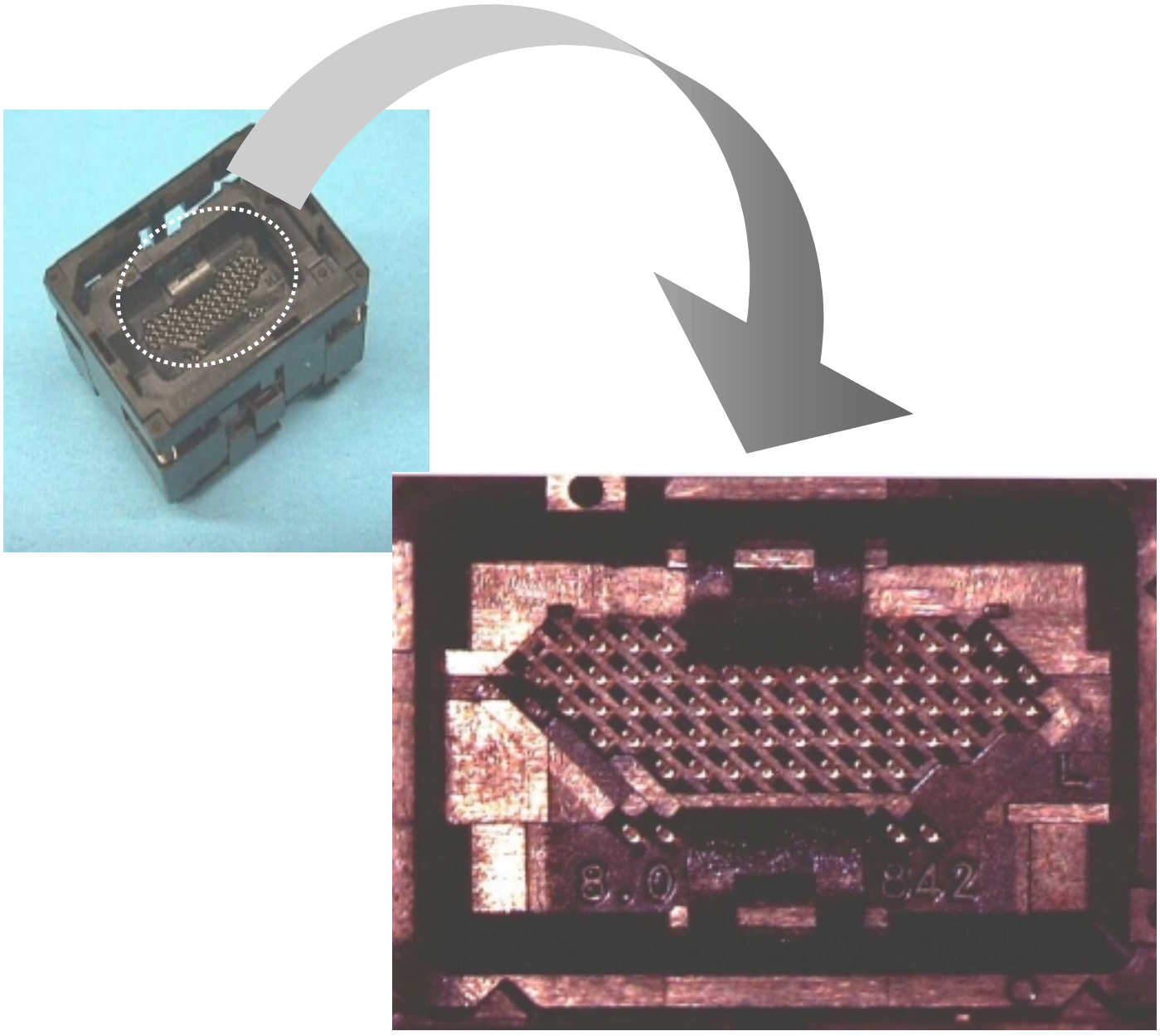


Figure 7: Schematic of the available space for actuation of the contact for a 0.5mm pitch array:
a) Actuation parallel to the array – interference
b) Actuation at 45º to axis of array.

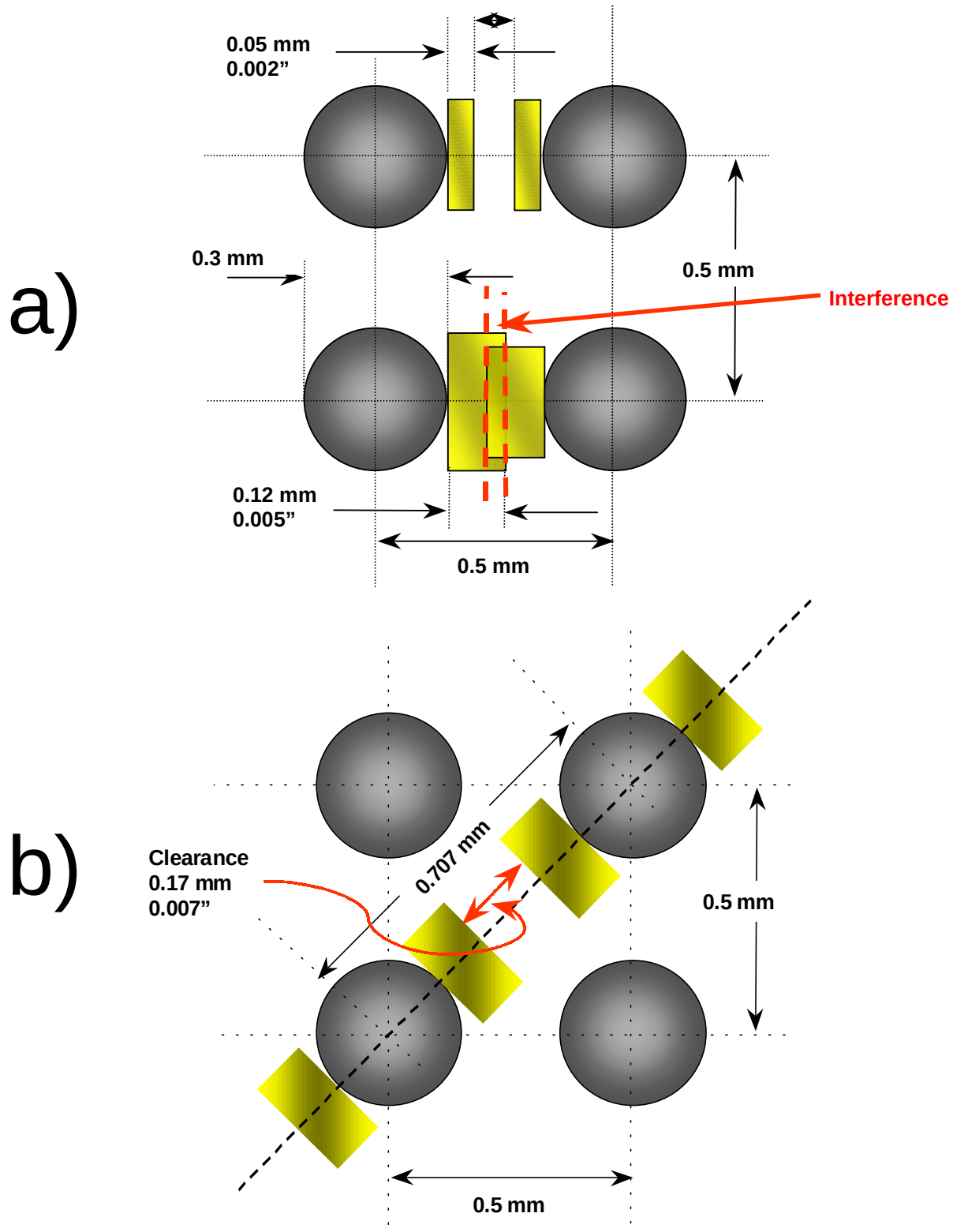
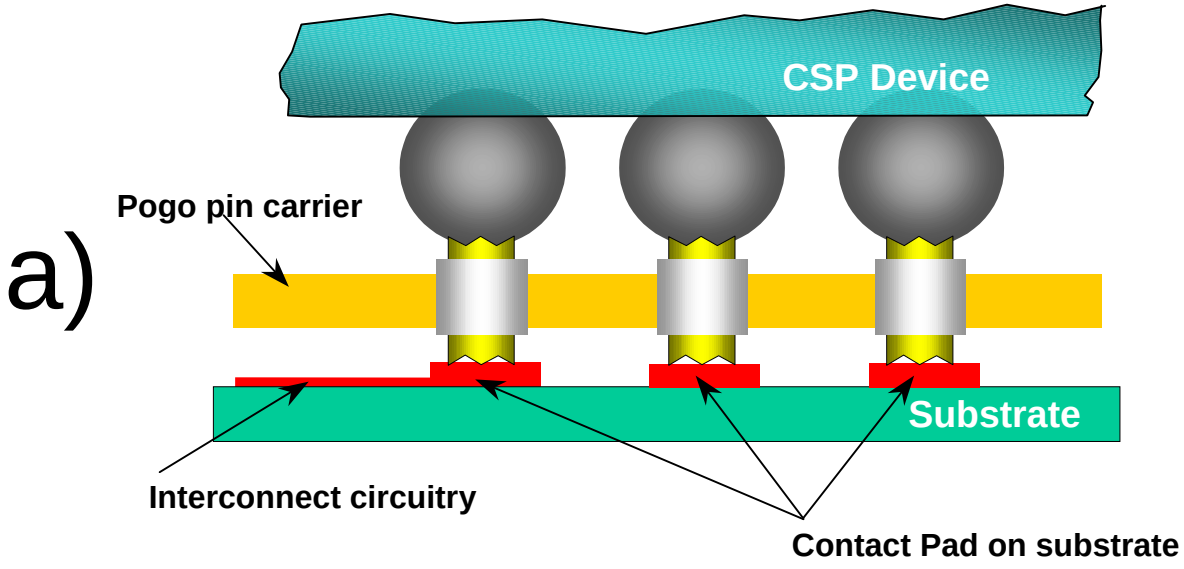


Figure 8: Schematic of two ideas being pursued for contacting solder balls at pitches of 0.5mm.
a) Pogo pin b) Spring



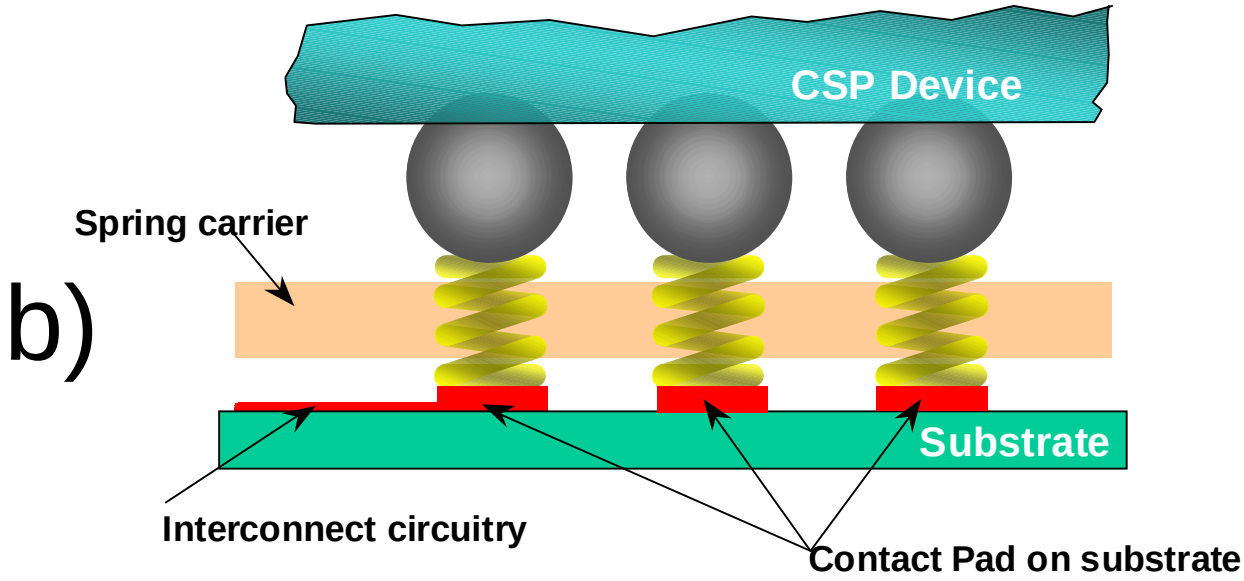
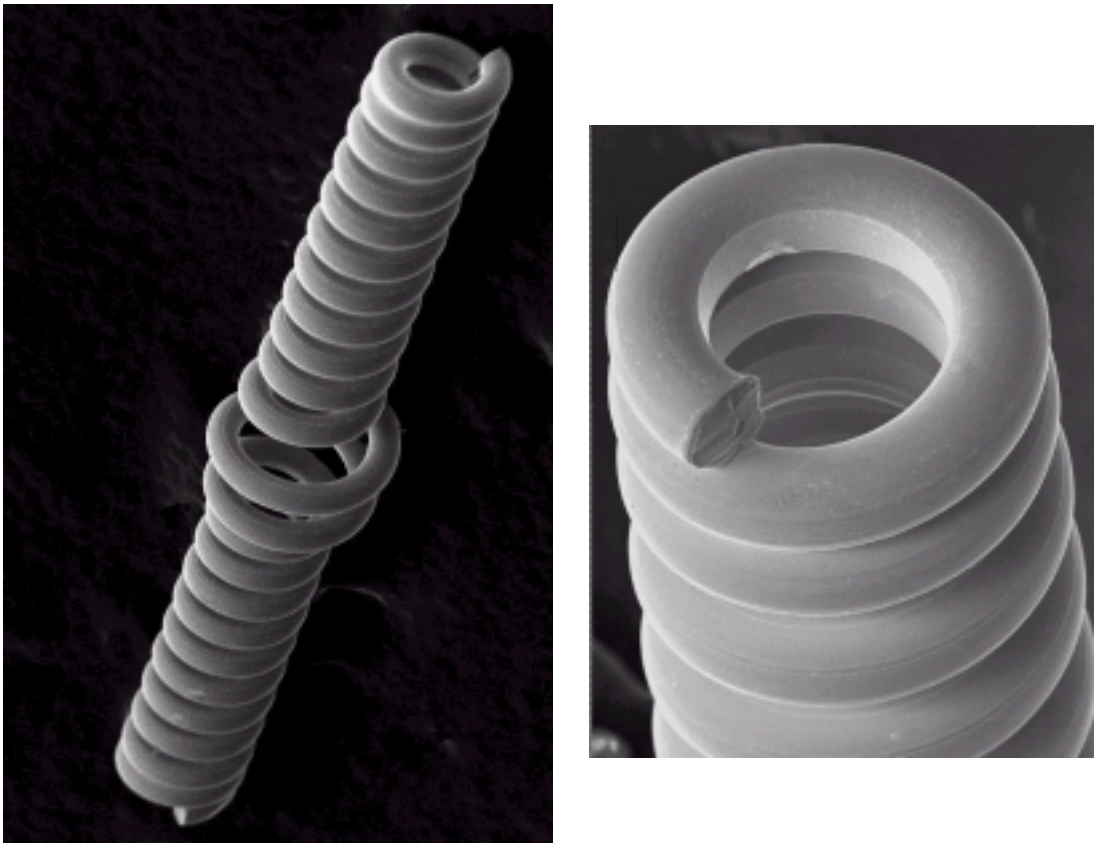


Figure 9: SEM Photographs of a custom spring used for contacting solder balls on a 0.5mm pitch CSP.
a) Overall photograph of spring b) Close up of end of spring



a) b)

Figure 10: A photograph of the clamshell style socket and part of the array of springs in the carrier.

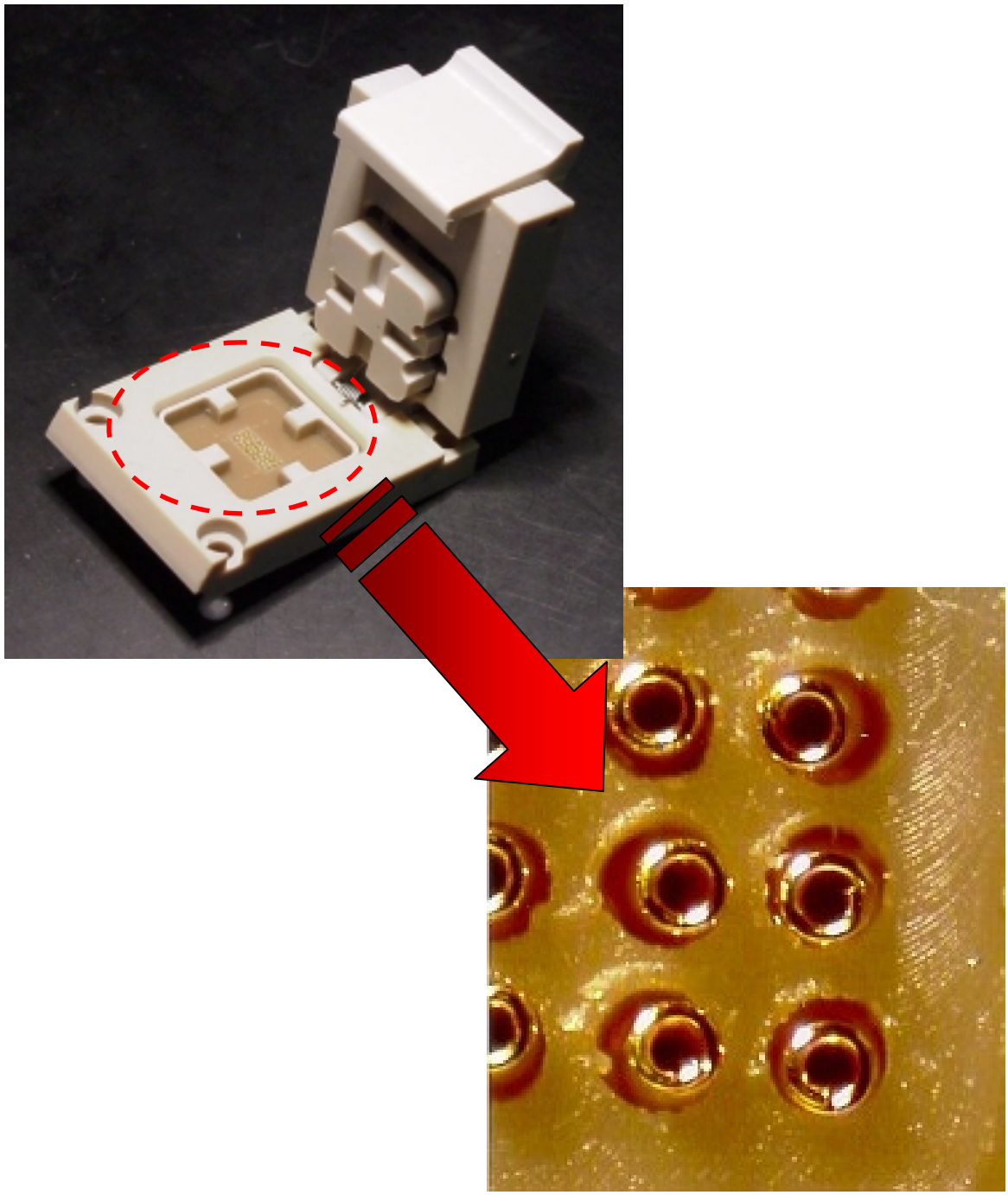


Figure 11: Cross-section through socket showing springs contacting a row of 14 solder balls on 0.5mm pitch and close ups of the contact between the spring and the solder ball.

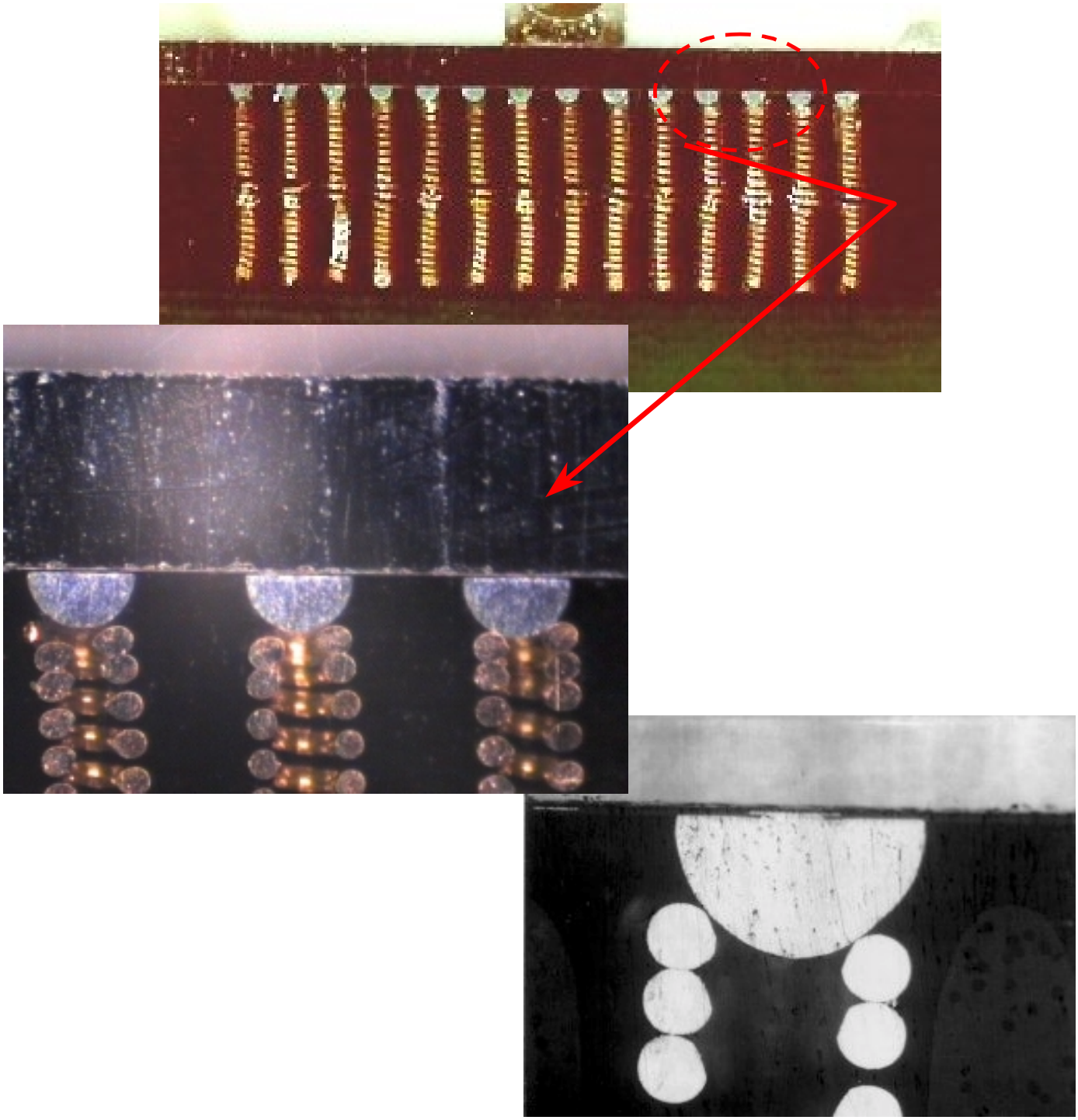


Figure 12: Probe marks on 0.5 mm array of solder balls after burn-in at 150ºC for 6 hours.